

**Quick Start Microsystems, LLC  
Getting Started Quickly in Microelectronics,  
Microsystems & Reliability Series**

# **21<sup>st</sup> Century Semiconductor Technology Handbook**

May 2009

**Ted Dellin, PhD  
Arlene Dellin, MS**  
[dellin@ieee.org](mailto:dellin@ieee.org)

*A fast, easy-to-understand way for people working in the industry to develop an intuitive understanding of:*

- *How microelectronic and optoelectronics devices work*
- *How ICs are fabricated*
- *What are the up-to-date challenges that are reshaping deep submicron microelectronics*

©2004-2009, Dellin, All Rights Reserved. Reproduction or distribution in any form is illegal and prohibited without express written permission.

**[www.quickstartmicro.com](http://www.quickstartmicro.com)**

### **Notice**

*This book is designed to rapidly introduce the basic ideas of microelectronics. As such it contains many simplifying assumptions and omissions. Furthermore, we cannot guarantee the accuracy of everything in this book. Therefore, it should be used for instruction, not to make manufacturing or other similar decisions.*

*The authors and publisher shall not be liable in any event for incidental or consequential damages based on, or relating to, any use of this book.*

**5/9/2009 4:11:00 PM**

# Table of Contents (Short)

## **MODULE I. INTRODUCTION**

- 1 Introduction
- 2 Economics and Industry Structure
- 3 Overview

## **MODULE II. SEMICONDUCTORS**

- 1 Intrinsic Semiconductors
- 2 Extrinsic Semiconductors
- 3 Currents in Semiconductors
- 4 pn Junctions
- 5 Metal/Semiconductor Junctions and Heterojunctions

## **MODULE III. METAL OXIDE SEMICONDUCTOR**

- 1 MOS Capacitor
- 2 MOS Transistor
- 3 Scaling
- 4 Non-Ideal Effects

## **MODULE IV. INTEGRATED CIRCUITS**

- 1 Integrated Circuits
- 2 Packaging

## **MODULE V. BASIC PROCESSES**

- 1 Starting Material
- 2 Defect Reduction
- 3 Lithography
- 4 Planarization
- 5 Doping
- 6 Deposition
- 7 Etching

## **MODULE VI. MOS PROCESSING**

- 1 Process Integration
- 2 Process Flow

## **MODULE VII. RELIABILITY**

- 1 Yield, Reliability and Quality

## **MODULE VIII. FUTURE TRENDS**

- 1 Future Trends
- 2 New Devices

## **MODULE IX. OPTOELECTRONICS**

- 1 Photo Diodes and Solar Cells
- 2 LEDs, Laser Diodes and VCSELs

## **GLOSSARY**

## **APPENDIX I: PHYSICAL CONSTANTS, METRIC PREFIXES & SYMBOLS**

## **APPENDIX II: THE BASIC EQUATIONS OF DEVICE PHYSICS**



# Table of Contents (Detailed)

## **MODULE I. INTRODUCTION**

### **I.1. Introduction**

1. The Silicon Miracle
2. A Brief History of Microelectronics
  - 2.1 The Invention of the Transistor
  - 2.2 1950s Laying The Foundation for Integrated Circuits
  - 2.3 The Invention of the Integrated Circuit
  - 2.4 The Foundations of Faster, Better, Cheaper
  - 2.5 The Evolution of Technology
  - 2.6 The Development of the Industry
  - 2.7 Lessons Learned From History
3. The Moore's Law Cycle That Has Driven The Industry
  - 3.1 The Start of the Cycle: Investing in the Next Generation.
  - 3.2 The Middle of the Cycle: Faster, Better, Cheaper ICs
  - 3.3 The End of the Cycle: The Economic Payoff
4. The Future: A Period of Unprecedented Change
  - 4.1 Future projections
  - 4.2 The Moore's Law Cycle Is Under Attack
  - 4.3 "Rumors of my death have been greatly exaggerated."
  - 4.4 "Decade of Unprecedented Change"
  - 4.5 A Possible Future Scenario
  - 4.6 Microsystems

### **I.2 Economics and Industry Structure**

1. Introduction
2. Economics 101
3. Income: Selling Chips
  - 3.1 Boom and Bust
  - 3.2 Selling Price of ICs
  - 3.3 Time is Money I
4. Expenses
  - 4.1 The Rising Cost of IC Factories: Moore's 2<sup>nd</sup> Law
  - 4.2 Time is Money II
  - 4.3 The Rising Cost of Problems: Dellin's Law
5. Changing Industry Structure
  - 5.1 Fabless Design Houses and (Design-less) Foundries
  - 5.2 Complete Solution Equipment Suppliers
6. System on a Chip (SOC)
7. Reducing the cost per transistor

### **I.3. Overview of CMOS**

1. Introduction
2. Semiconductors

3. Semiconductor Devices
  - 3.1 Junctions and Diodes
  - 3.2 The Transistor is a Device to Control Currents
  - 3.3 Review of Electric Circuit Concepts
  - 3.3 Only Two Things™
  - 3.4 MOS Transistor
  - 3.5 Scaling
4. Integrated Circuits
5. Processing
  - 5.1 Processing Hierarchy
  - 5.2 Unit Processes
  - 5.3 Process Modules and Process Integration
  - 5.4 CMOS Technology
6. “The Big Picture”

## **MODULE II. SEMICONDUCTORS**

### **II.1. Intrinsic Semiconductors**

1. Introduction
2. Crystals
3. The Silicon Crystal
4. Conduction and Valence Bands
5. Electrons and Holes in Semiconductors
  - 5.1 Thermal Generation of Electron Hole Pairs
6. Number of Electrons and Holes
7. Location of Electrons and Holes
6. Generation and Recombination

### **II.2 Extrinsic Semiconductors**

1. Extrinsic (Doped) Semiconductors
2. n Type Semiconductor
3. p Type Semiconductor
4. The Electron Hole Product
  - 4.1 The Number of Electrons and Holes in n and p type Semiconductors
5. Compensation and Counter Doping
6. Effect of Temperature on Carrier Concentrations
7. Resistivity
8. Degenerately Doped Semiconductor
9. The Fermi Level

### **II.3. Currents in Semiconductors**

1. Currents
2. Diffusion Currents
3. Drift Currents
4. Mobility

4. Universal Mobility Curves for Transistors
5. The Einstein Relationship Between Drift and Diffusion

#### **II.4. pn Junctions**

1. Junctions
2. pn Junctions: The Basic Building Block of Semiconductor Devices
3. The Unbiased pn Junction
  - 3.1 Forming the pn Junction
  - 3.2 Features of the pn Junction
  - 3.3 One-sided Junctions
4. The pn Junction with an External Voltage Applied
  - 4.1 Minority Carrier Injection and Extraction
  - 4.2 Junction Switching Speed
  - 4.3 Currents in One-Side Junctions
5. Reverse Bias Leakage Currents
6. Depletion Widths Determine The Minimum Size Of Transistors
7. Junction Breakdown

#### **II.5. Metal/Semiconductor Junctions and Heterojunctions**

1. Metals and Semiconductors
2. Work Function
3. The Metal Semiconductor Junction
4. Making Good Electrical Contact to Semiconductors
5. Heterojunctions

### **MODULE III. METAL OXIDE SEMICONDUCTOR**

#### **III.1. MOS Capacitor**

1. Introduction
2. MOS Capacitor
3. Threshold Voltage
  - 3.1 Flat Band Voltage
  - 3.2 Adjusting The Threshold Using Ion Implantation
  - 3.3 Temperature Dependence of the Threshold
4. CV Curves

#### **III.2. The Ideal MOS Transistor**

1. Introduction
2. The n Channel Transistor Will Be Studied
3. The Transistor's Geometry
4. The Transistor Has Four Electrical Connections
5. Applying Voltage to the Transistor With No Current Flow
6. Applying Both a Gate & Drain Voltage
7. Linear Current Region of Transistor Action
8. Saturation Current Region of Transistor Operation

9. Using Substrate (Back Gate) Bias To Change Threshold Voltage
10. Subthreshold Currents

### **III.3. Scaling**

1. Introduction
2. Ideal, Constant Field Scaling
3. Real World Scaling
4. Some Things Get Worse With Scaling

### **III. 4 Non-Ideal Effects**

1. Introduction
2. Short Channel Effect
3. Tunneling through the gate oxide
4. Velocity Saturation
5. Electrical Thickness of Gate Insulator

## **MODULE IV. INTEGRATED CIRCUITS**

### **IV.1 Integrated Circuits**

1. Introduction
2. A Simple Model for IC Performance
3. Parasitics
  - 3.1 Sources of Parasitic Resistance and Capacitance
  - 3.2 Source and Drain Parasitics
  - 3.3 Interconnect Parasitics
4. Cross Talk
5. A Simple Model for IC Power
6. Tradeoffs: Power versus Performance
  - 6.1. The need for tradeoffs
  - 6.2 Power versus performance

### **IV.2 Packaging**

1. Introduction
2. Packaging and Assembly
  - 2.1 Die Separation
  - 2.2 Mounting Die
  - 2.3 Wire Bonding
  - 2.4 Plastic Encapsulation
  - 2.5 Ceramic Packages
3. Package Types
4. Flip Chip and Ball Grid Array
5. Multiple Die in a Package

## **MODULE V. BASIC PROCESSES**

### **V.1 Starting Material**

1. Amorphous, Crystalline and Polycrystalline Materials
2. Specifying Crystal Planes and Directions: Miller Indices
3. The Diamond and Quartzite Crystal Structures
4. Surfaces of Crystals
5. Importance of Crystal Orientation
6. Crystal Growing
7. Epitaxial Wafers
8. Silicon on Insulator (SOI)

### **V.2 Controlling Defects and Contamination**

1. Three-Part Strategy
2. Reducing particles and contaminants
3. Cleaning
4. Gettering

### **V.3 Photolithography: Patterning Features**

1. Introduction
2. Masks
3. Process Flow
4. Photoresist (PR)
5. Resolution and Depth of Focus
6. Exposure Systems
7. Sub-wavelength Lithography

### **V.4 Planarization and Chemical Mechanical Polishing (CMP)**

1. Planarization: Removing Unwanted Topography
2. Reflowing glass
3. Etch back
4. Chemical Mechanical Polishing (CMP)
  - 4.1 CMP Challenges
  - 4.2 Post CMP Cleaning

### **V.5 Doping (Implant and Diffusion)**

1. Doping
2. Ion Implantation
  - 2.1 Range and Straggle
  - 2.2 Channeling
  - 2.3 Implant Damage and Annealing
3. Diffusion
  - 3.1 Qualitative Description of Diffusion
  - 3.2 Simple Analytical Solutions

### **V.6 Thin Films: Oxidation and Deposition**

1. Deposition: Adding Thin Films
2. Thermal Growth
  - 2.1 Thermal Oxidation
  - 2.2 Using Silicon Nitride as a Thermal Oxidation Mask
  - 2.3 Segregation of Dopants During Oxidation
  - 2.4 Silicides
3. Chemical Vapor Deposition (CVD)
  - 3.1 Plasma Enhanced CVD (PECVD)
  - 3.2 High Density Plasma CVD
  - 3.3 Atomic Layer Deposition
  - 3.4 Epitaxial Si
  - 3.5 Polysilicon
  - 3.6 CVD Oxides
  - 3.7 CVD Silicon Nitride
  - 3.8 CVD Tungsten (W)
4. Physical Vapor Deposition (PVD)
5. Electroplating
6. Spin on Films

## **V.7 Etching**

1. Etching
  - 1.1 Isotropic vs. Anisotropic Etching
  - 1.2 Etch Selectivity
  - 1.3 Using a Hard Mask
2. Wet Etching
3. Plasmas
4. Dry Etching
  - 4.1 Etching High Aspect Ratio Vias: Sidewall Polymers
  - 4.2 Macro-Loading and Micro-Loading
  - 4.3 Etching Oxides
  - 4.4 Etching Polysilicon
  - 4.5 Etching Al
  - 4.6 Plasma Charging Damage
5. CMP Etching in Damascene Process

## **MODULE VI. MOS PROCESSING**

### **VI.1. CMOS Process Integration**

1. Introduction
2. Potential Parasitic Leakage Current Paths
3. Wells
  - 3.1 Single Well vs. Dual Well (Twin Tub)
  - 3.2 Forming the Well by Drive In or By High Energy Implant
4. Isolation
  - 4.1 Guard Bands

- 4.2 LOCOS (Local Oxidation of Silicon)
- 4.3 Shallow Trench Isolation (STI)
- 5. Gate Stack
  - 5.1 P+ vs. N+ Polysilicon Gates for PMOS
- 6. Source and Drain
- 7. Electrical Contact to Silicon
- 8. Multilevel Metalization
  - 8.1 Aluminum and Copper
  - 8.2 Dielectric Between Metal Lines
- 9. Passivation and Bondpads
- 10. Process Integration

## **VI.2. CMOS Technology Process Flow**

- 1. Introduction
- 2. CMOS Process Flow
- 3. Front End of Line (FEOL)
  - 3.1 Starting Wafers
  - 3.2 Mask 1: Shallow Trench Isolation (STI)
  - 3.3 Mask 2: P Wells and Mask 3: N Wells (“Twin Well/Twin Tub”)
  - 3.4 Gate Insulator
  - 3.5 Mask 4: Polysilicon Gate
  - 3.6 Mask 5: n Channel Shallow Source/Drain Extensions
  - 3.7 n Channel HALO (or Pocket) Implants
  - 3.7 Mask 6: n Channel Shallow Source/Drain Extensions
  - 3.8 n Channel HALO (or Pocket) Implants
  - 3.9 Gate Sidewall Spacer
  - 3.10 Masks 7 and 8: Deep Source and Drain Regions
  - 3.11 Comparison of Epi and SOI Wafers After FEOL
- 4. Back End of Line (BEOL)
  - 4.1 SALICIDE (Self Aligned Silicide)
  - 4.2 Mask 9: Interlevel Dielectric and Contact Cut
  - 4.3 Contact Metalization
  - 4.4 Mask 10: Metal 1 (M1)
  - 4.5 Masks 11 and 12: Metal 1/Metal 2 Via and Metal 2
  - 4.6 Terminology
  - 4.7 Masks 13-20: Rest of Vias and Metal Levels
  - 4.8 Mask 20: Bond Pad and Passivation
- 5. Copper Metalization
- 6. Bond Pads and Passivation

## **MODULE VII. RELIABILITY**

### **VII.1 Reliability, Yield & Quality**

- 1 The Most Important Thing
- 2 Yield
- 3 Reliability

- 4 IC Failure Modes
  - 4.1 Dielectric Breakdown
  - 4.2 Hot Carrier Degradation
  - 4.3 Electromigration
  - 4.4 Stress Voiding
5. Quality

## **MODULE VIII. FUTURE TRENDS**

### **VIII.1. Future Challenges and Potential Solutions**

1. Introduction
2. Technical Challenges
  - 2.1 Device Physics Challenges
  - 2.2 Processing Challenges
3. New Materials
  - 3.1 Cu Interconnect
  - 3.2 Low k Interlevel Dielectrics
  - 3.3 High k gate insulators
  - 3.4 Strained Silicon
4. New Devices
5. Design Challenges
6. Reliability Challenges
7. Economic Challenges
8. Timetable for Changes: International Technology Roadmap for Semiconductors (ITRS)

### **VIII.2 New Devices**

1. Introduction
2. Multiple Threshold Voltages
3. Silicon on Insulator (SOI) Transistors
  - 3.1 Partially Depleted vs. Fully Depleted
  - 3.2 Partially Depleted SOI
  - 3.3 Fully Depleted SOI
4. Multi-gate MOS Transistors
5. Novel transistors

## **MODULE IX. OPTOELECTRONICS**

### **IX.1 Photo Diodes & Solar Cells**

1. Introduction
2. Light
3. Direct and Indirect Bandgap Semiconductors
4. Light Absorption

- 4.1 Light Absorption in Direct Bandgap Semiconductors
- 4.2 Light Absorption in Indirect Bandgap Semiconductors
- 4.3 High Energy Photons are Less Efficient
- 5. Photodiode
  - 5.1 Spectral Response
- 6. Photovoltaics
  - 6.1 Solar Cells

## **IX.2 LEDs, Laser Diodes and VCSELS**

- 1. Introduction
- 2. Spontaneous Emission
- 3. Stimulated Emission
- 4. Forward-Biased Diode as a Light Emitter
  - 4.1 Double Heterostructure
- 5. Light Emitting Diode
- 6. Laser Diode
- 7. VCSEL
- 8. Comparison of LED, Laser Diode and VCSEL

## **GLOSSARY**

## **APPENDIX I: PHYSICAL CONSTANTS, METRIC PREFIXES & SYMBOLS**

## **APPENDIX II: THE BASIC EQUATIONS OF DEVICE PHYSICS**

## **About the authors**

*Dr. Theodore (Ted) Dellin retired as the Chief Scientist of the Microelectronics and Microsystems Center at Sandia National Laboratories in Albuquerque, New Mexico. After retirement, Dr. Dellin founded Quick Start Micro Training LLC ([quickstartmicro.com](http://quickstartmicro.com)) to provide training in microelectronics, reliability and microsystems. He leads the development of the reliability section of the International Technology Roadmap for Semiconductors, is a member of the Sematech Reliability Technical Advisory Board and is a past Chair of the IEEE Nonvolatile Memory Technology Workshop. He has taught short courses for organizations in the U.S. and Europe and has given many tutorials at the IEEE International Reliability Physics Symposium. Dr. Dellin has a PhD in physics from the City University of New York.*

*Arlene Dellin, M.S., is a learning specialist. She has worked as a learning diagnostician and has taught at the Junior College level. She has a B.S. in Psychology from Hunter College and a M.S. in Learning Disabilities from the University of the Pacific.*

## **Acknowledgements**

*Mike Strizich of Analytical Solutions, Inc. ([www.analyticalsolutions.com](http://www.analyticalsolutions.com)) provided many of the excellent SEM cross sections used throughout this Handbook.*

*We have had the privilege to work with, and learn from, an exceptional set of colleagues at:*

*Sandia National Laboratories*

*Sematech Reliability Technical Advisory Board*

*International Technical Roadmap for Semiconductors*

*and many other industrial, academic and government organizations*

*These colleagues provided invaluable insights into the technology and business of semiconductors that are reflected in this handbook.*

## **Notice**

*The images from IBM used in this book are all courtesy of IBM and unauthorized use is prohibited. The same applies to all other organizations that provided images for this book.*