The End Gate of Moore's Law Seminar

May 15, 2007

Quick Start Micro Training LLC
www.quickstartmicro.com

The End Game of Moore's Law: 2007 Update

Dr. Ted Dellin

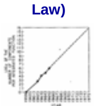
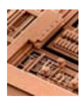
dellin@ieee.org, 1-505-401-8707
Quick Start Micro Training, LLC, www.quickstartmicro.com
Reliability Lead, Intl. Tech. Roadmap for Semiconductors (ITRS)
Member, Reliability Council, Sematech
Chief Scientist (Retired) of the Microsystems Center, Sandia Natl. Lab

Material is from Meeting the Submicron CMOS Challenge, Semiconductor Technology and IC Reliability Short Courses.

Outline

- **Background on Moore's Law and Scaling**
- **The technical challenges and current/potential solutions**
- **The economic challenge**
- **The future of Moore's Law and what this means for IC users**

Key Milestones In the History of Integrated Circuits

1947 First Transistor	1958 Planar Process (Si, SiO_2, Al)	1959 First Integrated Circuit	1965 More Transistors Per IC (Moore's Law)	1972 Scaling for Faster ICs	●●●	1998 Replacing Planar Process Begins
				"Design of MOSFETS … With Very Small Dimensions"		
Bardeen, Brittain & Noyce Bell Labs	Noyce & Hoerni, Fairchild	Kilby, TI	Moore, Fairchild Electronics Magazine	Denard et al, IBM		IBM Introduces Cu Metalization

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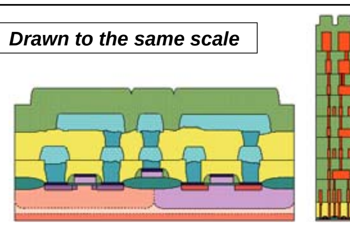
Denard et. al.: Scaling Down Results In Faster, Better and Cheaper ICs

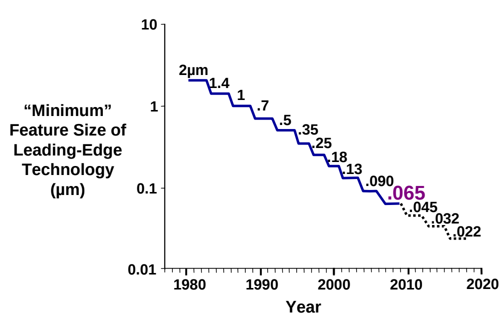
Drawn to the same scale



1.0µm (Mid-1980s)	0.10µm (Early 2000's)
~100,000's Transistors	~100,000,000's Transistors
Speed ~ 10 MHz	Speed ~ 3,000 MHz
~0.1 ¢ / transistor	~0.00005 ¢ / transistor

Figure: Sematech

Every 2-3 Years The Industry Has Introduced A New Technology Generation ("Node")



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Scaling Also Encounters Serious Problems Due to Physical and Material Limits

Scaling into the deep sub-micron region

Fundamental Physical and Material Limits

-Large Power Consumption

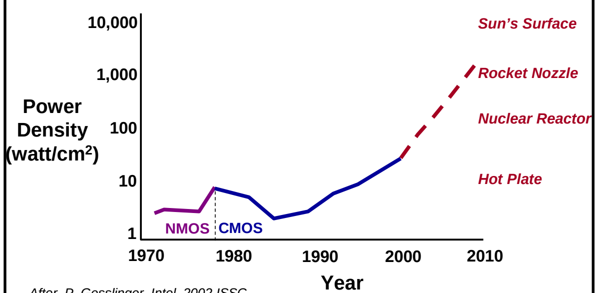
-Harder to Achieve Performance Gains

-Processing, Design, Reliability & Test Issues

5 Major, Interrelated, Technical Challenges

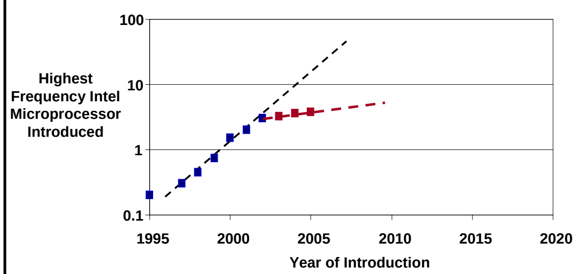
- Increasing Power Consumption
  - *Active power and (especially) stand-by power*
- Worsening Performance-Robbing Parasitics
  - *Negating the improvements in transistor speed*
- Processing Challenges
  - *Affordable, shorter wavelength lithography*
  - *Process integration of new materials*
  - *Increasing process variations*
- Design Challenge
  - *Harder and more expensive to successfully design custom ICs*
- Reliability Challenge
  - *Reduce reliability margins*
  - *Qualify new materials, devices and processes*

Example: Power Density Trend of Intel Microprocessors



After, P. Gesslinger, Intel, 2002 ISSC

Slowing Down (Essentially Stopping?) Microprocessor Speed Increases



http://www.intel.com/pressroom/kits/quickrefyr.htm

Reaction to the Growing Scaling Challenge

“No More Moore”

TJ Rogers, CEO, Cypress Semiconductor

“Scaling is Dead”

Bernie Meyerson, CTO, IBM

EETIMES

Texas Instruments Exits Process Development Race

1/24/07

The Future of Moore’s Law

“No exponential is forever…

but forever can be delayed”

Gordon Moore, 2003 ISSC Conference

How long can we sustain Moore’s Law in high volume production?

Even if we can, is it affordable?

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We Need to Reinvent Microelectronics To Sustain The Moore's Law Cycle

Scaling into the deep sub-micron region

Fundamental Physical and Material Limits

-Large Power Consumption

-Harder to Achieve Performance Gains

-Processing, Design, Reliability & Test Issues

Replace Almost All of the Traditional Materials Used In ICs

New Device Structures

Design for Manufacturing (Litho, Process Variability, ...)

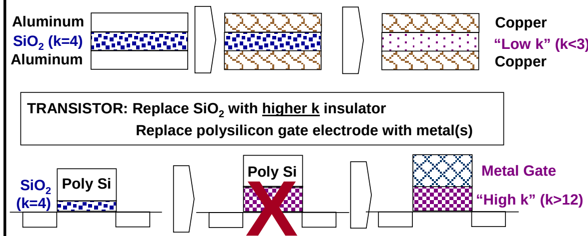
.....

????

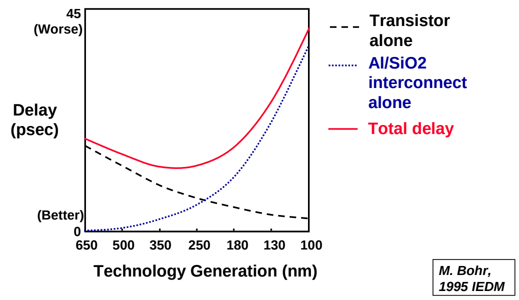
2 Major Material Changes: *Interconnect and Transistor*

INTERCONNECT: Replace Al with Cu
Replace SiO_2 with lower k insulator

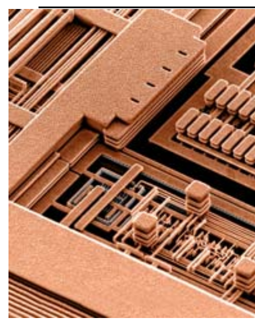
TRANSISTOR: Replace SiO_2 with higher k insulator
Replace polysilicon gate electrode with metal(s)



Interconnect Is Becoming Increasingly Important in Determining Delay Time



Copper



Courtesy of IBM

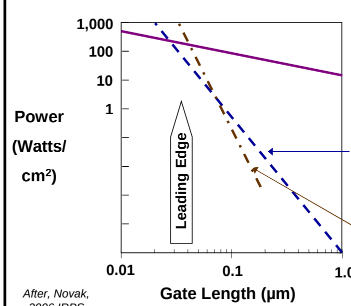
- Copper has a lower resistivity than Al
- Less signal delay on wiring – faster ICs
- Copper has been successfully introduced into volume manufacturing
- Concerns with continued scaling of copper
  - *Increase in resistivity*
  - *Decrease in electromigration lifetime*

As The Intermetal Dielectric Constant Is Reduced Other Properties Are Degraded

GOOD NEWS	BAD NEWS			
Dielectric Constant	Mechanical Strength	Adhesion	Electric Breakdown Strength	Thermal Conductivity
Improves IC Speed & Reduces Crosstalk	*More Mechanical Failures (Cracking, Delamination)*		*Worse Electrical Breakdown*	*Higher On Chip Temperature*
	Worse Electromigration			*Worse Electromigration*

Unlike copper, Implementation of low k proved to be very difficult

Active, and Especially Standby, Power Has Increased Sharply With Scaling



Active Power
(Scaling down IC voltage more slowly than dimensions)

Standby Power Due to Subthreshold Leakage
(Scaling down threshold voltage)

Standby Power Due to Gate Oxide Tunneling
(Scaling down gate insulator thickness)

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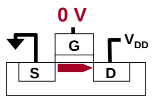
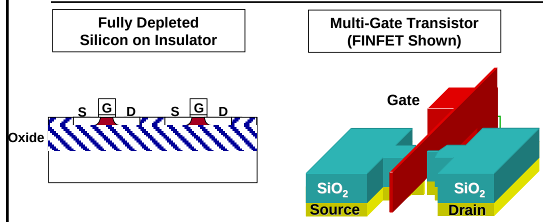
Subthreshold Leakage Current Increases Exponentially With Scaling



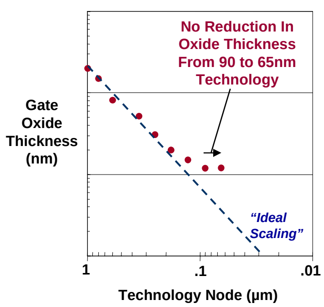
- We need to reduce the threshold voltage when we scale to produce faster transistors
- Subthreshold leakage increases exponentially as the threshold voltage is scaled down
  - *Tradeoff: We need to reduce threshold voltage to get faster ICs*
- Fundamental physics tells us we will always have a minimum amount of subthreshold leakage

Advanced Device Structures Can Reduce Subthreshold Leakage Currents

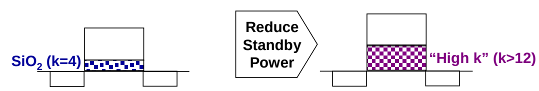


- Can come much closer to minimum subthreshold leakage limit
- Not in production – serious processing challenges

Growing Gate Tunneling Currents Have Led to End Of Oxide Scaling

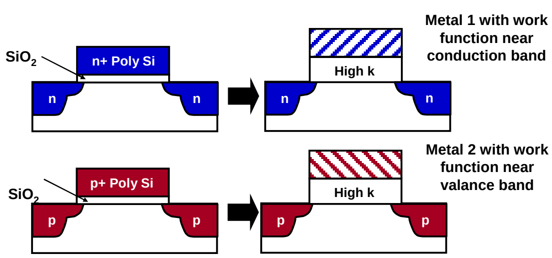


To Reduce Standby Power SiO_2 Needs to Be Replaced with a New "High k" Dielectric



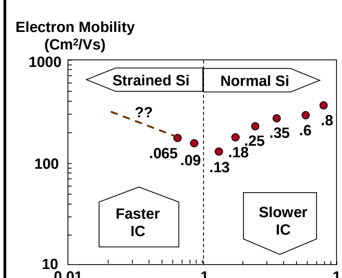
- "k" is the dielectric constant
- Replacing SiO_2 (k=4) with a higher k material can reduce tunneling currents without affecting transistor current
- Probably the most difficult of all changes

High k and Metal Gate Need To Be Introduced At the Same Time

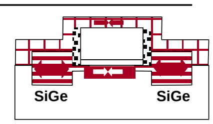


- Difficult to find metals with the right work functions.
- Significant process integration and reliability challenge
- So far, no company has introduced high k/metal gate into production

Use of "Strained Silicon" Has Increased Mobility and IC Speed



After S. Thompson, et. al., Intel TJ, May 2002 and P. Bai, 2004 IEDM



- Silicon channel of MOS transistor is strained
- Results in higher mobility and thus faster ICs
- Has allowed manufacturers to
  - *Stop scaling down gate oxide*
  - *Delay the introduction of high k gate insulators*

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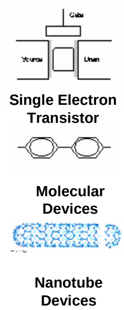
We Are On The Verge of The Most Significant Material Change

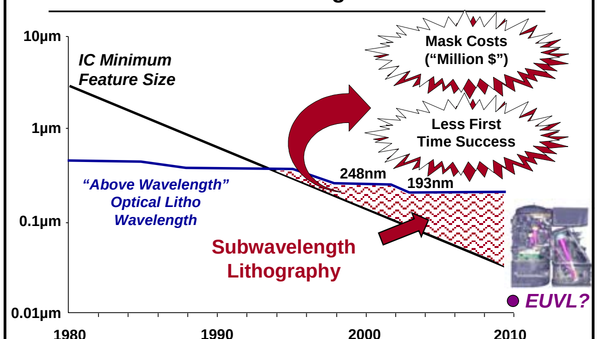
- The need to replace SiO_2 with a high k alternative dielectric is arguably the most significant material change in the history of ICs
- The experience replacing SiO_2 between metal lines with a low k insulator shows how difficult a material change can be
- It seems that the industry will be forced to make this change next year when moving to 45nm

What About The Use of Non-CMOS, Novel Devices to Extend Scaling?

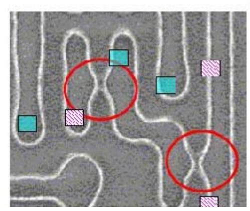


- Since 2001 the International Technology Roadmap for Semiconductors (ITRS) has been systematically looking at novel devices
- Conclusions:
  - *For digital logic applications nothing is better than CMOS*
  - *However, novel devices may have an impact on memories and specialized applications (vision)*

Subwavelength Lithography Comes At a High Price



wysiNwyg: What You See is NOT What You Get



Bridging defect due to pattern sensitivity of optical proximity correction (Madge, LSI Logic)

- Optical proximity correction is required for subwavelenght litho
- However, it is hard to accurately predict
  - Sensitive to local pattern
  - Sensitive to variations in mask features and in wafer flatness
- These inaccuracies are discovered after part is fabricated
  - *Require a new design spin*

Submicron Design Challenges

- Increasing complexity
  - More transistors
  - Design has to fix power and processing problems
- Growing interaction between design and process is impacting yield and first-time success
  - Traditional design rules no longer guarantee yield
  - Hard to predict exact shape of features when using sub-wavelength lithography
  - Need to do statistical design to account for increasing processing variability
- Design (including mask) costs are escalating

A Growing Reliability Risk

- Stresses (fields, currents, temperatures) are increasing
- New materials, new processes and new devices can lead to new or changed failure mechanisms
- The ability to life-test and to screen-out defective parts is being reduced
- Tradeoffs between reliability, performance, power …. are becoming more difficult

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The Dollar Is Mightier Than The Electron

Economics, not physics, will probably be the determining factor in the future of the IC industry

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The "Just Enough," Application-Specific IC

- As tradeoffs become more difficult, it becomes harder to make a robust, one-size-fits-all technology
- Technology being optimized around the needs of major applications
- Need to produce the "Just Enough" IC that meets, but does not exceed, customer requirements
  - Tradeoffs are so challenging it is hard to just meet requirements
  - Exceeding requirements is an "opportunity cost" that should be avoided – use excess capability to give customer what it wants

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The IC Market Is Increasingly Dominated by Consumer Electronics

- Price sensitive
- Low profit margins
- Less funds available for R&D
  - Fixed percentage of profits
- Often require relatively shorter IC lifetimes

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Major Economic Challenges

- Finding "killer aps" that will pay a premium price for large volumes of ICs
  - *Don't want to be like DRAMS: from 1995-2001 doubled the bits shipped per year while total revenue fell from $45B to $10B***
- Factory costs (and everything else) double each new generation
- Escalating time and cost of developing custom chips
- Business case for the Research-Development-Application enterprise needed to have robust solutions for advanced technologies ready when needed

**S. Cullen, Electronic News. 1/14/02 p 20

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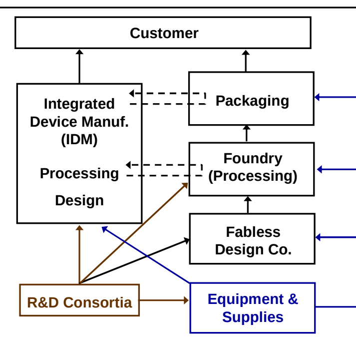
Major Players in the Global Microelectronics Industry



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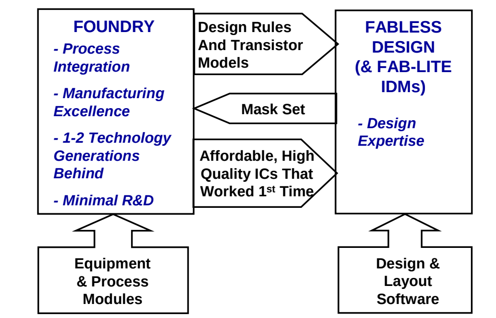
The Original (Ideal) Model for the Foundry & Fabless Business Case



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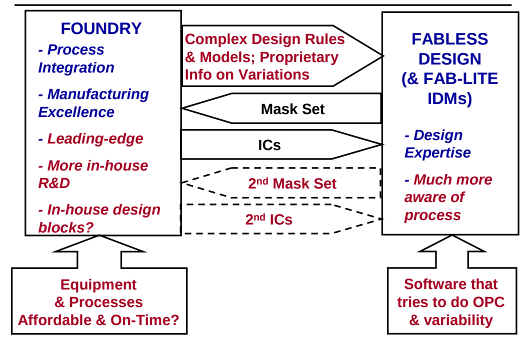
In My Opinion The Foundry/Fabless Model Is In Flux



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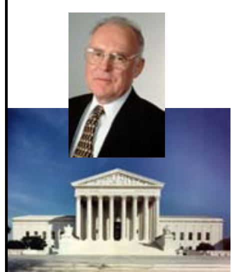
What Do We Mean By "Moore's Law"



- Strictly speaking it just refers to a doubling of transistors per IC every few years
  - *Satisfied even if speed does not increase*
  - *Basically controlled by manufacturability*
- Popularly, Moore's law is often thought to refer ICs that get exponentially faster, better and cheaper with time
  - *Historically, this required scaling to get faster transistors*
  - *Today, it may be accomplished with multi-cores, system in a package, …*
- "Moore's Law With Scaling" Is harder to sustain than "Moore's Law Limiting to More Transistors/IC"

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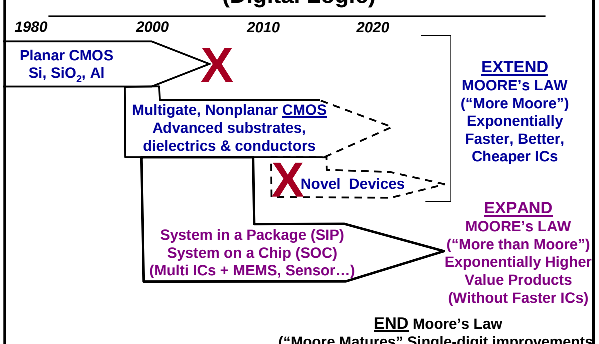
Possible Future Scenarios for Moore's Law (Digital Logic)



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My Free *(and worth every penny)* Predictions

- Moore's Law does not stop in the near future
  - *Innovation will just stay ahead of problems*
- However, only a decreasing number of users will be able to afford fully custom, state-of-the-art ICs
- More and more users will ***indirectly benefit*** from new technologies
  - *Economics (cost, time to market) will force the use of standard parts, structured ASICs and FPGAs*
  - *These ICs are not as good as a fully custom IC*
  - *But they will improve with each new technology node*
- Key to future of Moore's Law: Economics

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What Does This Mean for IC Users?

- It is going to be harder (not impossible) to successfully use new IC technologies due to:
  - *Difficult tradeoffs between power, performance, reliability …*
  - *Escalating cost and risk of developing fully custom ICs*
- Users of advanced ICs will need to:
  - *be much better informed about IC technologies*
  - *work more closely with IC manufacturers*

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Final Thoughts

- ICs were a dominant agent of change in the second half of the 20th Century
  - *Faster, better and cheaper*
  - *Widespread applications benefited from ICs*
  - *Generated a lot of productivity improvements and wealth*
- In the 21st Century ICs have/will become a less powerful agent of change
- What is the comparable next big thing that will reshape our world and when will it kick in?
  - *Will it be biotech, microsystems or nano be comparable? – perhaps*
  - *Will we have a "breather" before the next big thing? - likely*
  - *What does this mean for the U.S. economy and national security? – an important consideration*

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Summary

- Scaling down technologies to make faster, better and cheaper ICs is running into multiple roadblocks
- Need to "reinventing" the CMOS IC using new materials and new device structures
  - *Thing to watch: implementation of high k/metal gate transistors*
- Economic pressures are reshaping the industry
  - *Thing to watch: future of the Foundries*
  - *Thing to watch: the position of, and impact on, the U.S.*
- Moore's Law will continue in the near term, but fewer users will be developing fully custom ICs

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Acknowledgements

- I gratefully acknowledge the information I have learned from my colleagues at
  - ITRS Process, Integration and Device Structures (PIDS) Working Group, Chaired by Peter Zeitzoff, Sematech
  - Reliability Technical Advisory Board, Sematech
  - Sandia National Laboratories
- I also acknowledge the contribution of Arlene Dellin who helped make this material easier to understand

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For More Information

- A copy of the slides is at quickstartmicro.com
- 2005 International Technology Roadmap for Semiconductors http://public.itrs.net/
  - *2007 edition being developed*
- www.intel.com/research
- Short courses taught by the speaker in Albuquerque and in-house (www.quickstartmicro.com)
  - Meeting the Submicron CMOS Challenge Seminar
  - Integrated Circuit Reliability,
  - Semiconductor Devices With Optoelectronics
  - Semiconductor Technologies With MEMS

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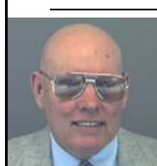
Speaker's Bio



Dr. Ted Dellin is the Chief Scientist (Retired) of the Microsystems Center at Sandia National Laboratories having retired from full time work after 35 years at Sandia. He still runs the Microsystems University that he established at Sandia. Dr. Dellin has led the development of the reliability section of the International Technology Roadmap for Semiconductors since the 1990s and is a member of the Sematech Reliability Technical Advisory Board. He is a past chair of the IEEE Nonvolatile Memory Workshop and has given 5 tutorials at the International Reliability Physics Symposium. He also teaches a series of short courses in microelectronics, devices, technology, submicron CMOS and reliability for organizations in the U.S. and Europe. He is a coauthor with Arlene Dellin of the 21st Century Semiconductor Technology Handbook and he contributed the Submicron CMOS chapter to the ASM Failure Analysis Desk Reference. Dr. Dellin has a PhD in physics from the City University of New York.

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